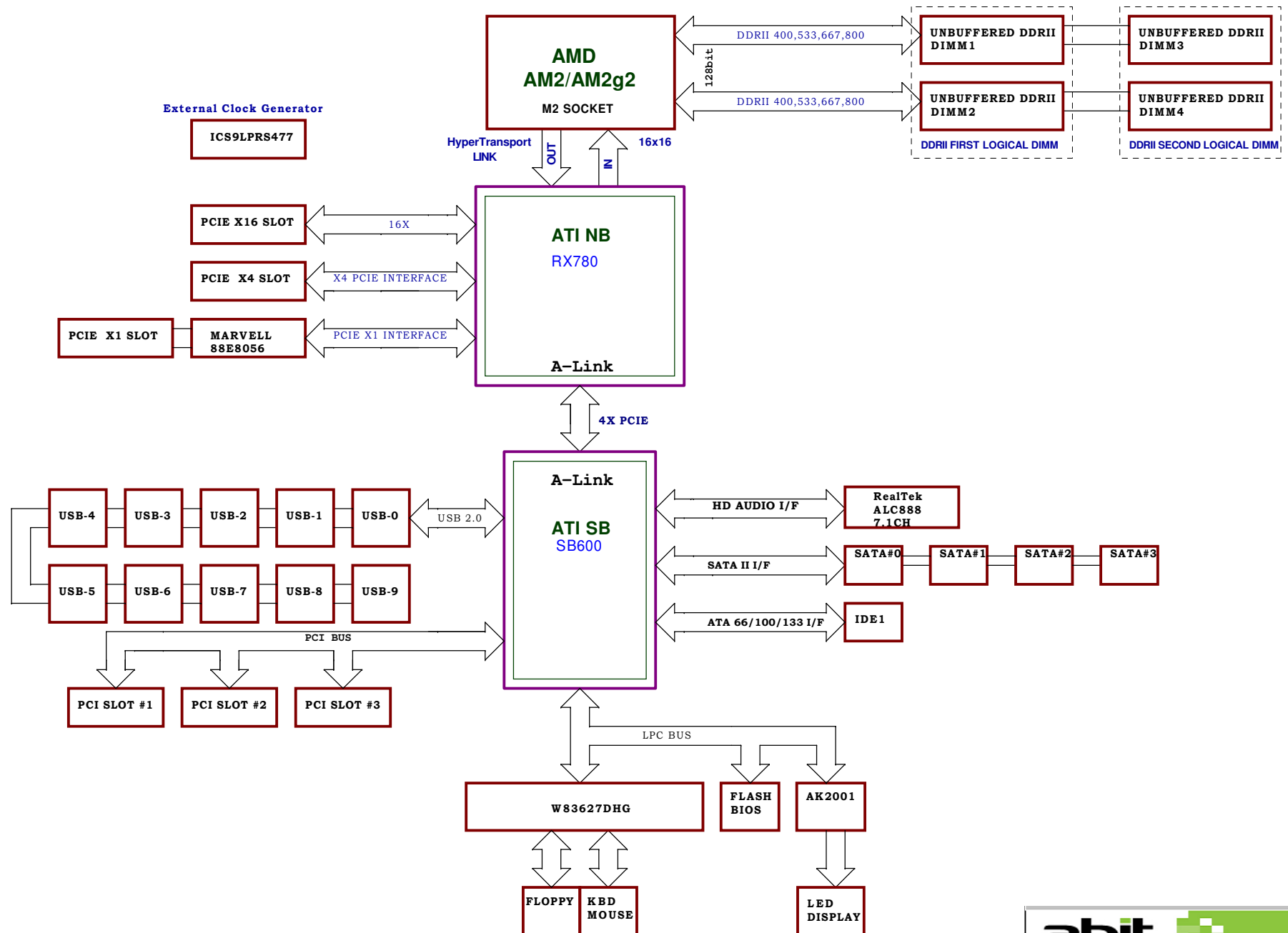
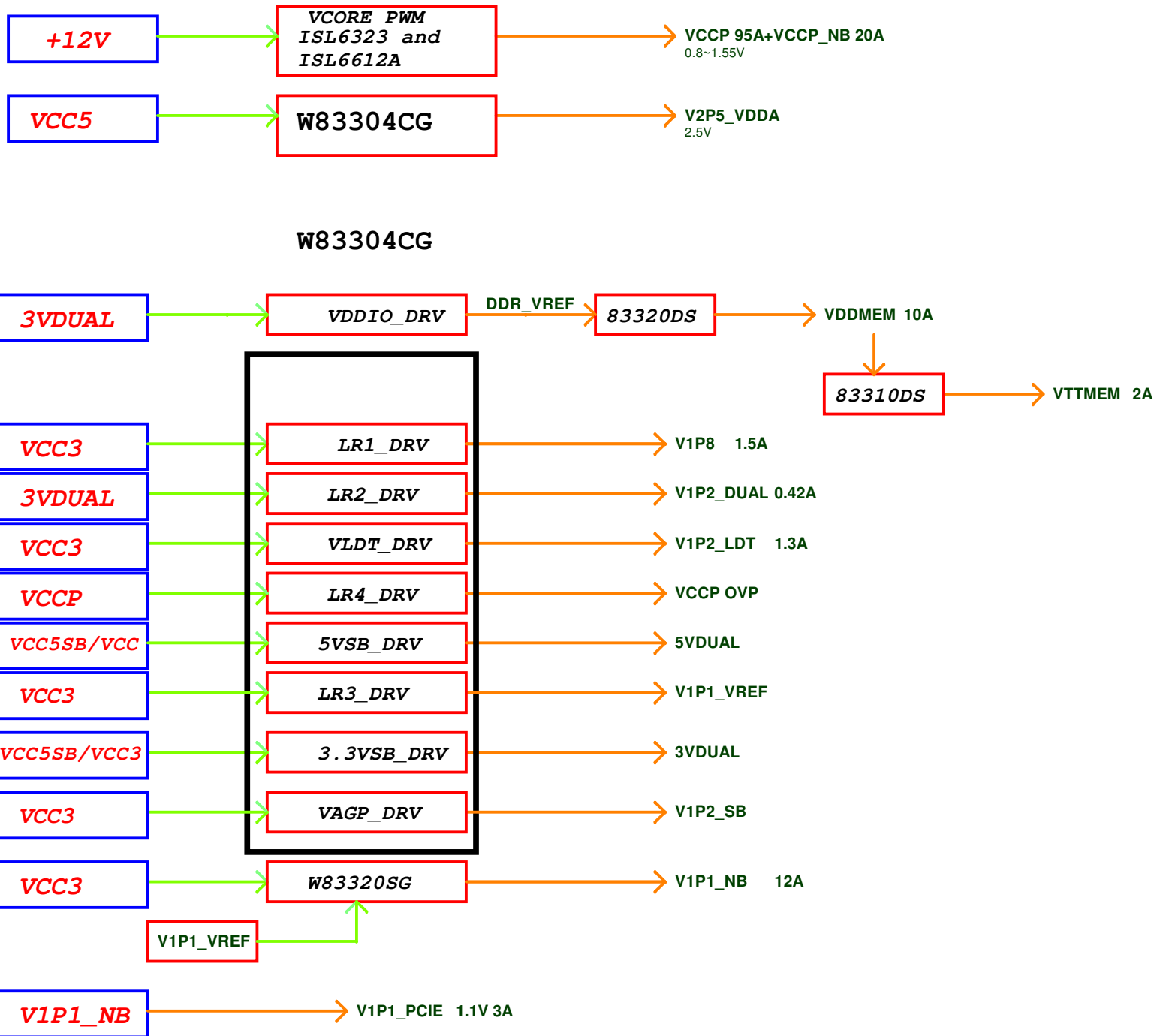


abit AX78 V0.2 SCHEMATICS

TITLE	SHEET
SYSTEM BLOCK DIAGRAM	2
POWER DISTRIBUTION	3
K8 CPU	4~8
DDR2 DIMM SOCKET	9~12
AMD RX780	13~15
CLOCK GEN.	16
PCI-E X16	17
PCI-E x4/x1	18
AMD SB600	19~22
PCI SLOT 1,2,3	23
SATAII 1-4 and IDE & AK2001	24
LPC I/O W83627DHG	25
FPIO , FWH , SMB ,FDC , ATX	26
KB , MS & FP-USB 1,2,3	27
HD-AUDIO ALC888	28
PCIE GbE LAN	29
FAN & HW MONITOR	30
PWM ISL6323 & ISL6613	31~32
W83304CG	33~34
MECHANICAL	35

U-ABIT AX78 BLOCK DIAGRAM



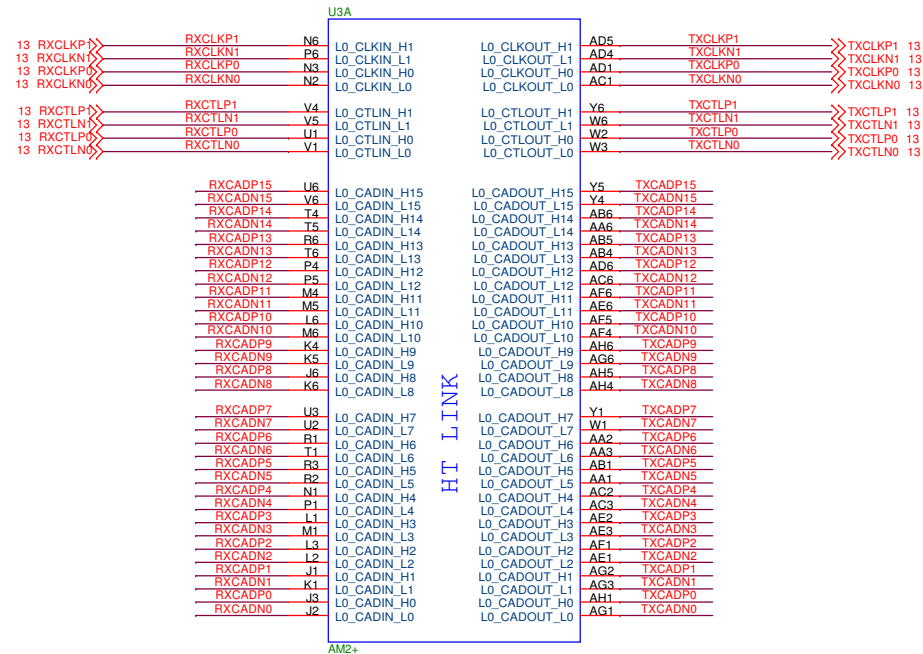


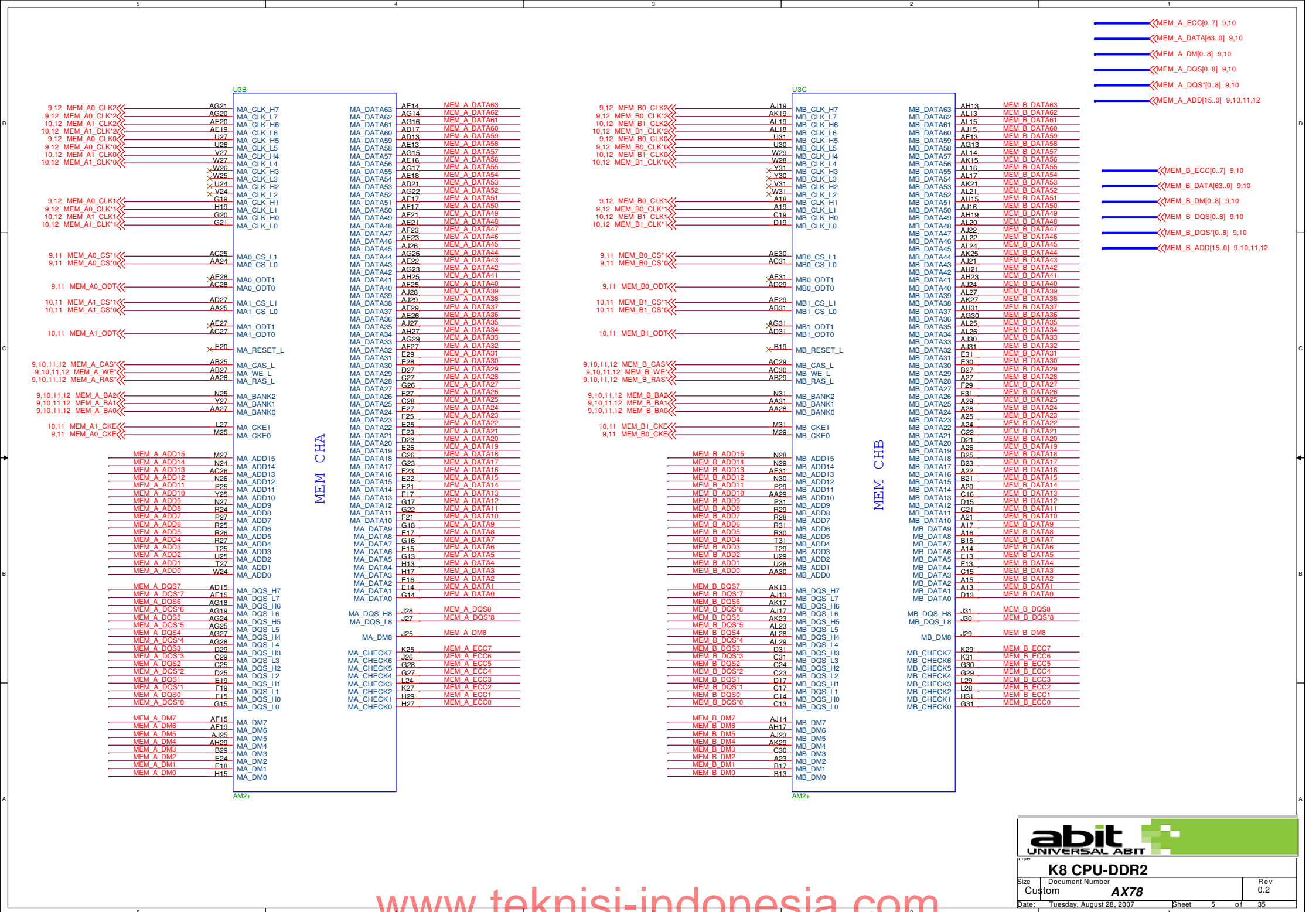
AMD M2 CPU	
VCCP	VDDCORE default 95A+20A
V2P5_VDDA	VDDA 2.5V 0.2A
VDDMEM	VDDIO 1.8V 10A
VTTMEM	VTT 0.9V 2A
V1P2_LDT	VLDT 1.2V 0.5A

NB RX780	
V1P2_LDT	VDDHT 1.2V 0.5A
1P1_PCIE	PCI-E CORE 1.1V 3A
V1P1_NB	NB CORE 1.1V 3A
V1P8	NB 1.8V 1.8V 0.6A
	PCI-E VDDA18 1.8V 0.9A

SB SB600	
1P2_SB	X4 PCI-E 1.2V 0.8A
1P2_SB	SATA I/O 1.2V 0.2A
1P2_SB	SATA PLL 1.2V 0.01A
1P2_SB	PCI-E PVDD 1.2V 80mA
1P2_SB	SB CORE 1.2V 0.6A
VCC3	3.3V I/O 3.3V 0.45A
3VDUAL	3.3V S5 PW 3.3V 0.01A
V1P2_DUAL	USB CORE I/O 1.2V 0.2A
V1P2_DUAL	1.2V S5 PW 1.2V 0.22A

<<TXCADP[15..0] 13
 >>RXCADP[15..0] 13
 <<TXCADN[15..0] 13
 >>RXCADN[15..0] 13







11 HUG

K8 CPU-DDR2

Size

Document Number

Rev

Custom

AX78

0.2

Date:

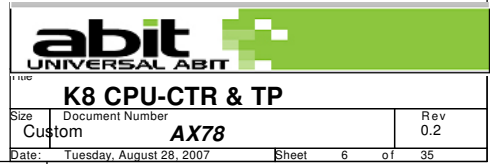
Tuesday, August 28, 2007

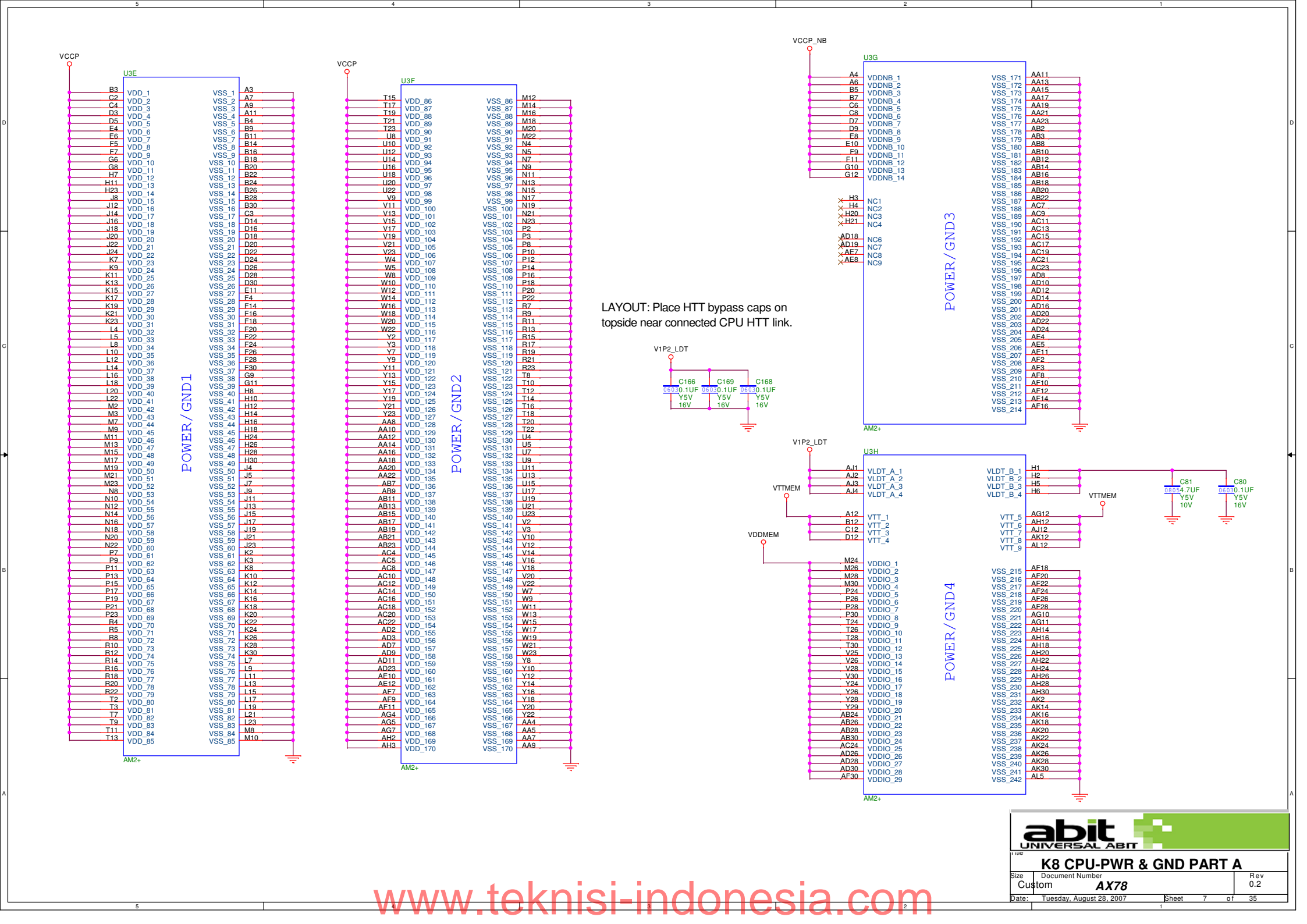
Sheet

5

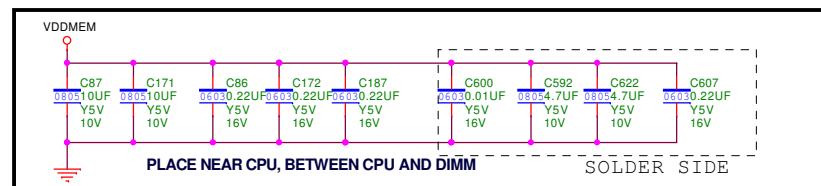
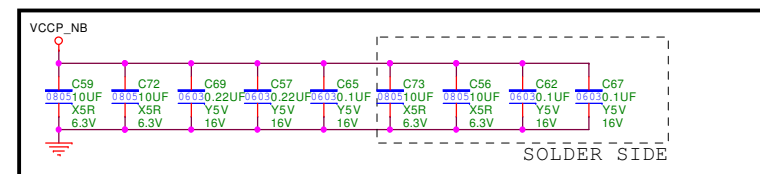
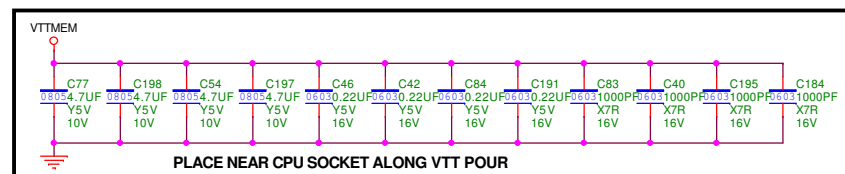
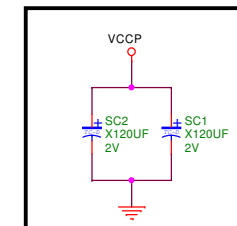
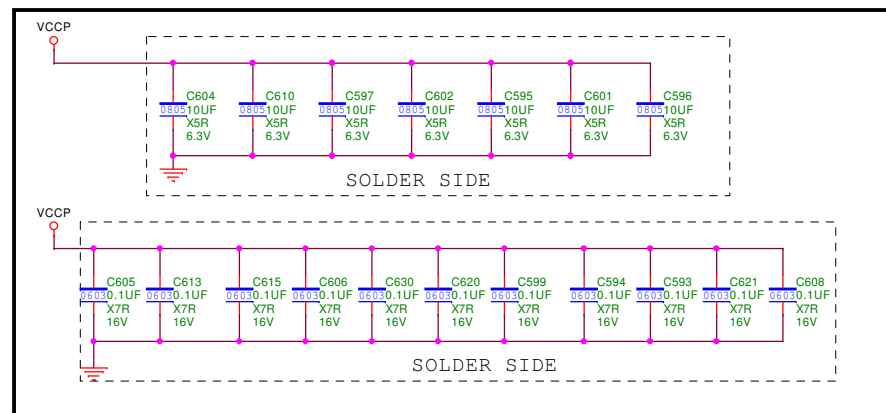
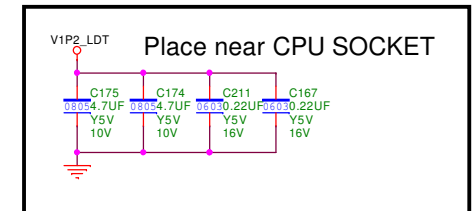
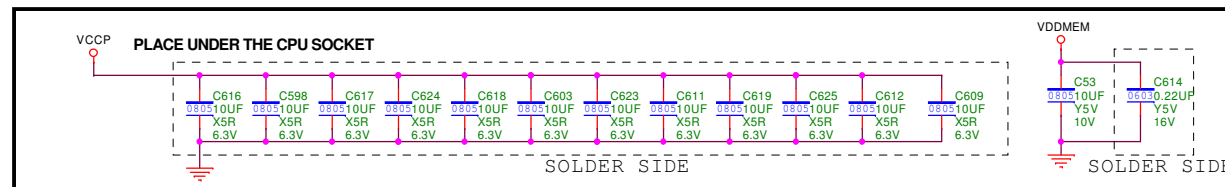
of

35



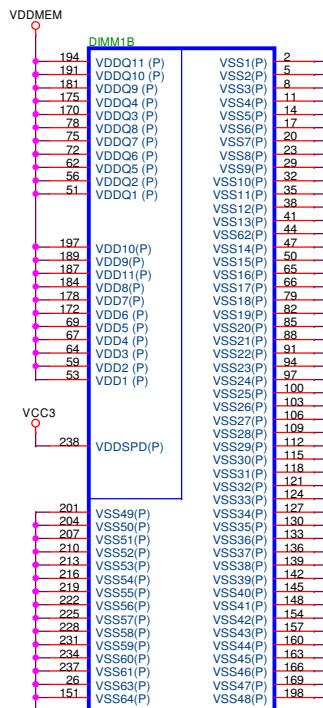


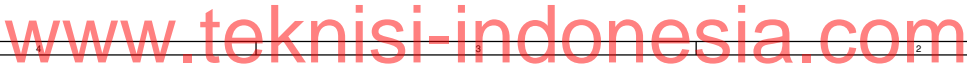
Bottomside Decoupling

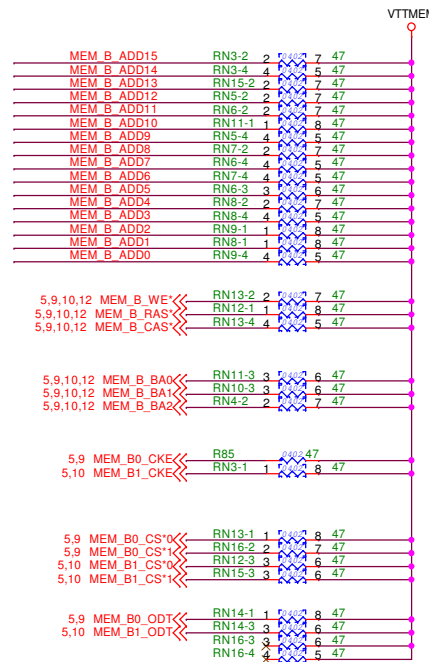
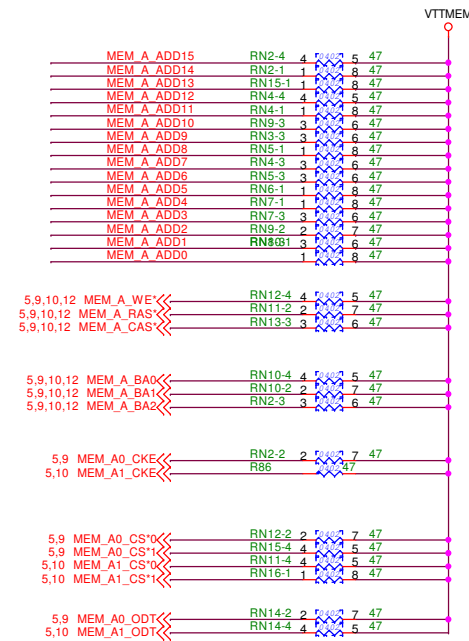
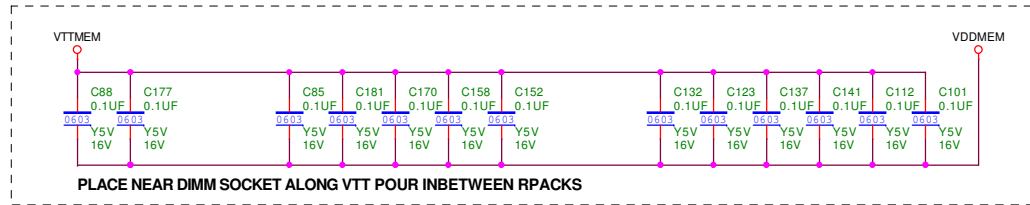
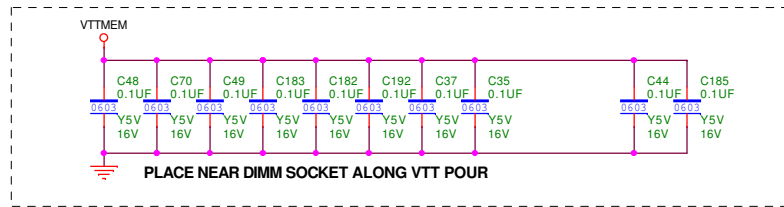


MEM_A_ECC[0..7] 5,10
MEM_B_DATA[63..0] 5,10
MEM_A_DM[0..8] 5,10
MEM_A_DQS[0..8] 5,10
MEM_A_ADD[15..0] 5,10,11,12

MEM_B_ECC[0..7] 5,10
MEM_B_DATA[63..0] 5,10
MEM_B_DM[0..8] 5,10
MEM_B_DQS[0..8] 5,10
MEM_B_ADD[15..0] 5,10,11,12

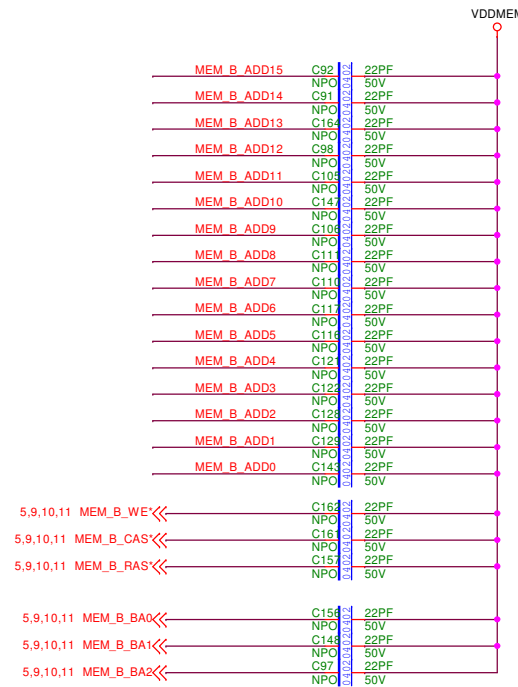
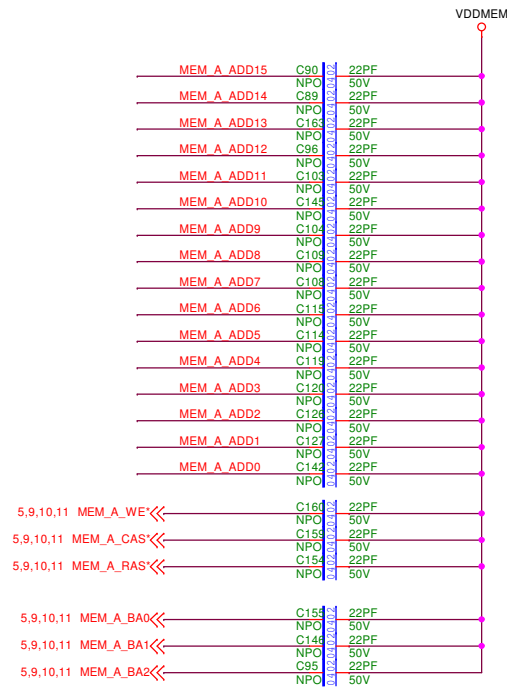






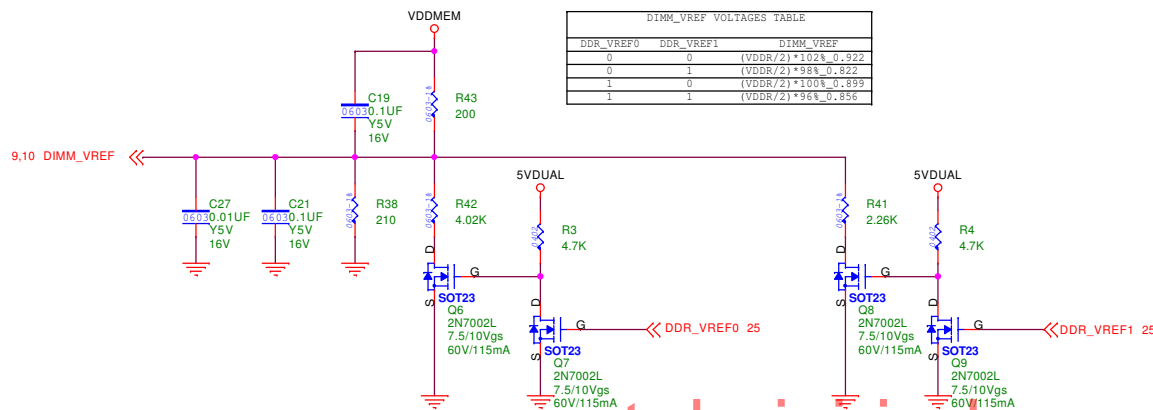
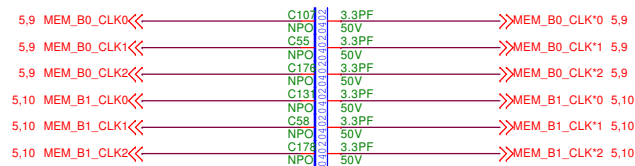
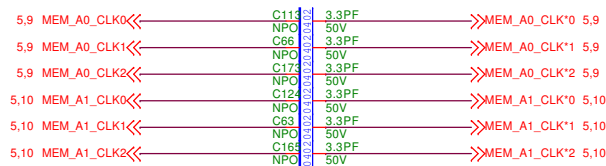
MEM_A_ADD[15..0] 5,9,10,12

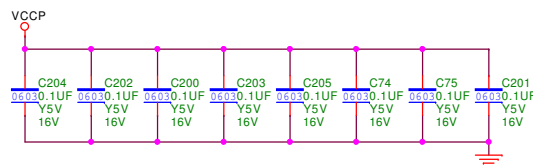
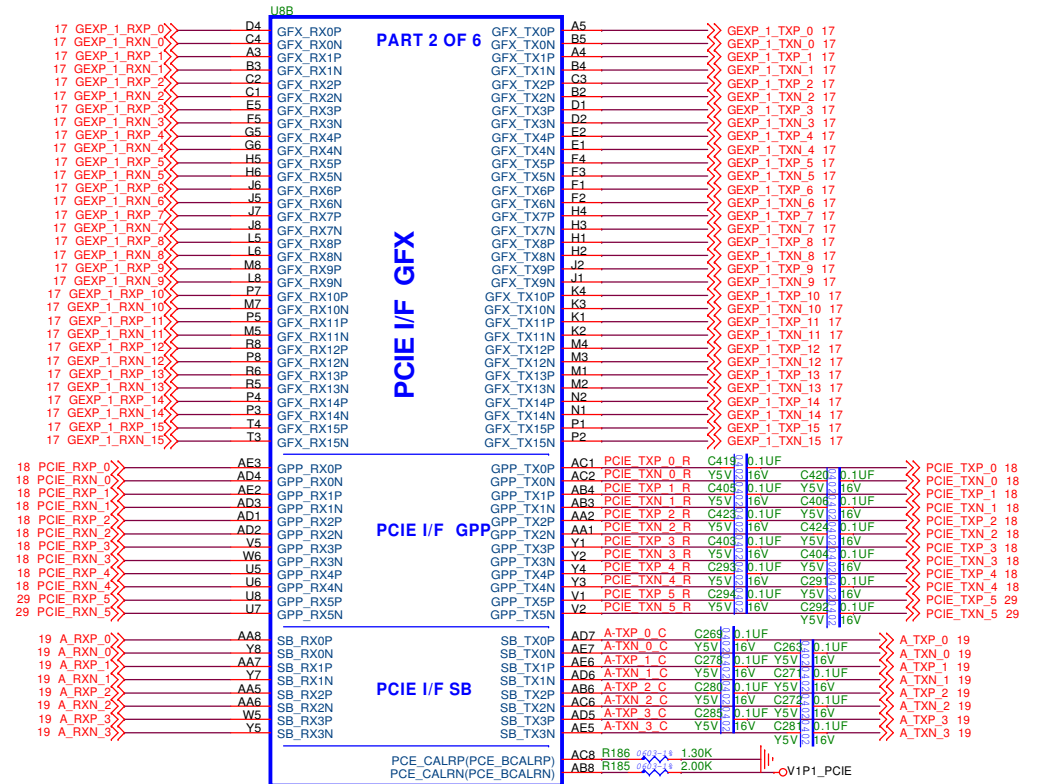
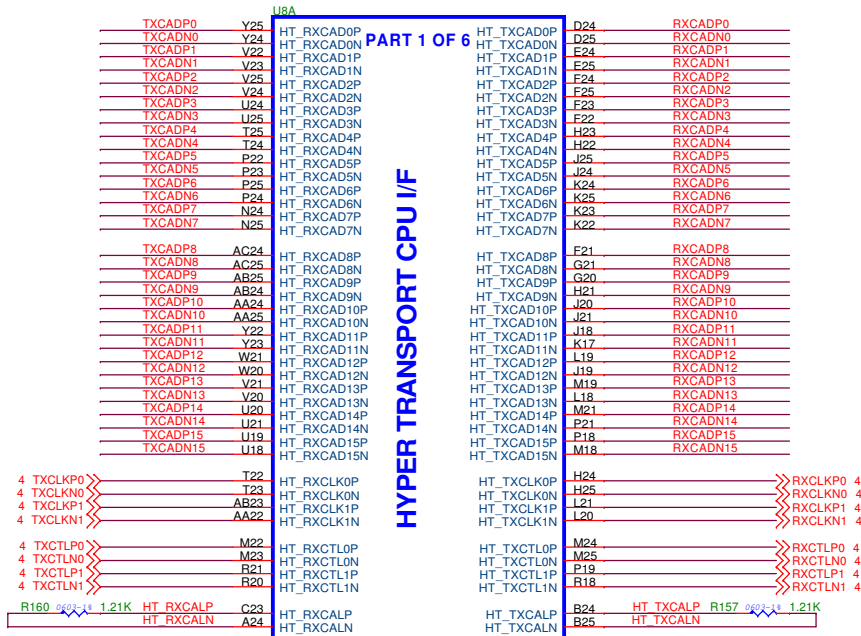
MEM_B_ADD[15..0] 5,9,10,12

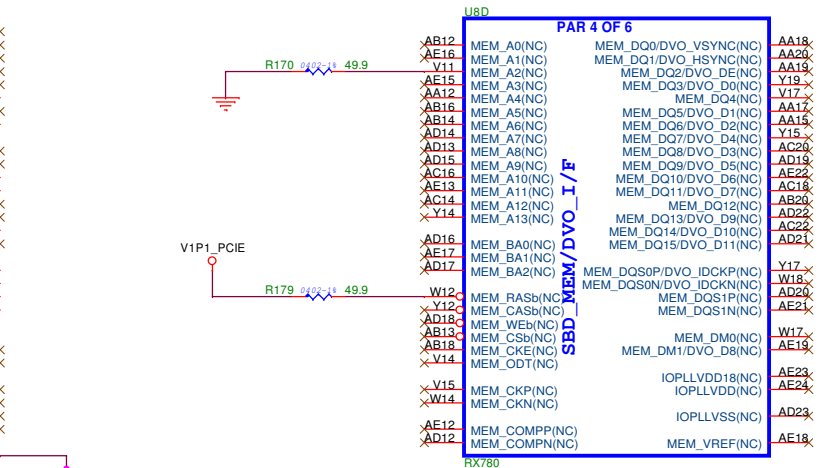
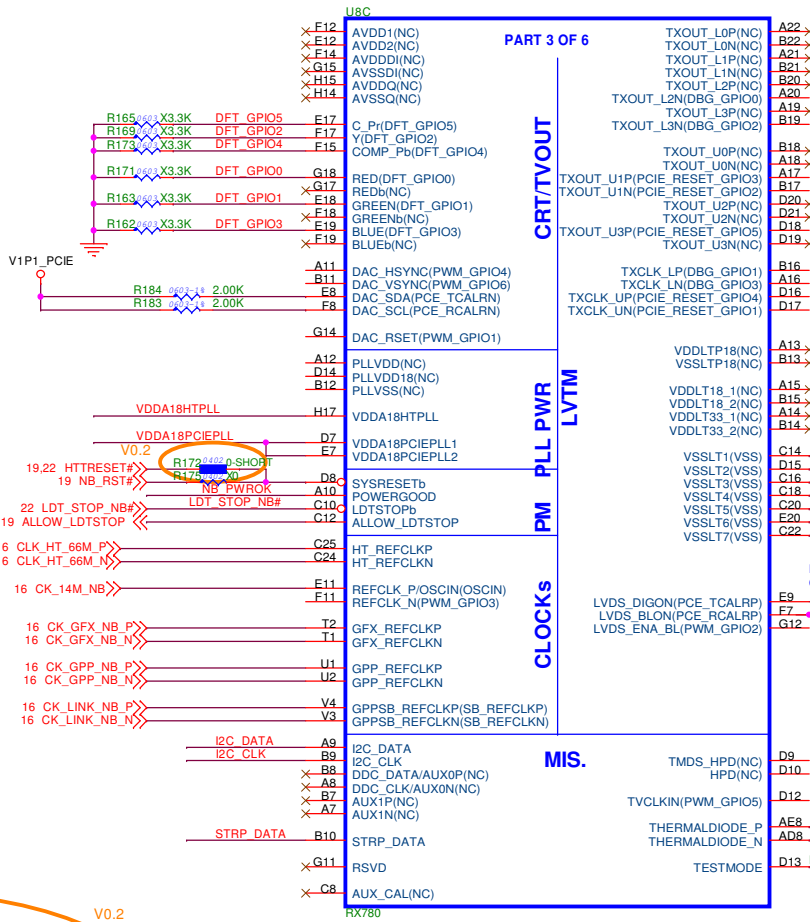
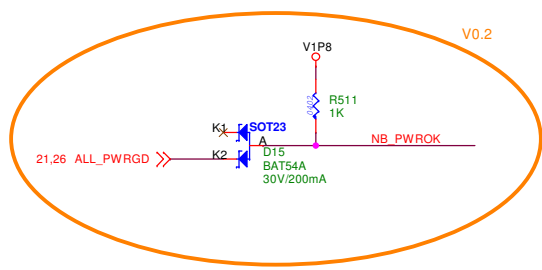
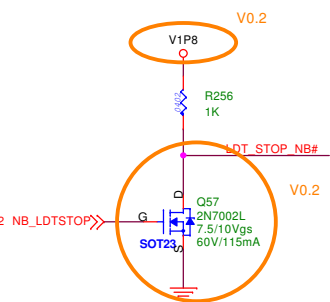
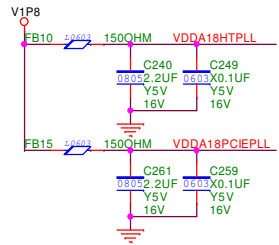


MEM_A_ADD[15..0] 5,9,10,11

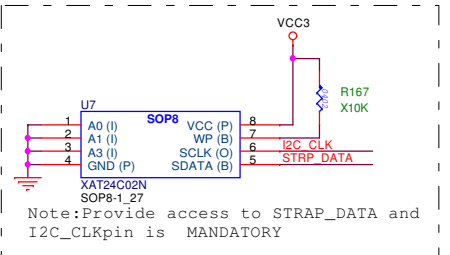
MEM_B_ADD[15..0] 5,9,10,11



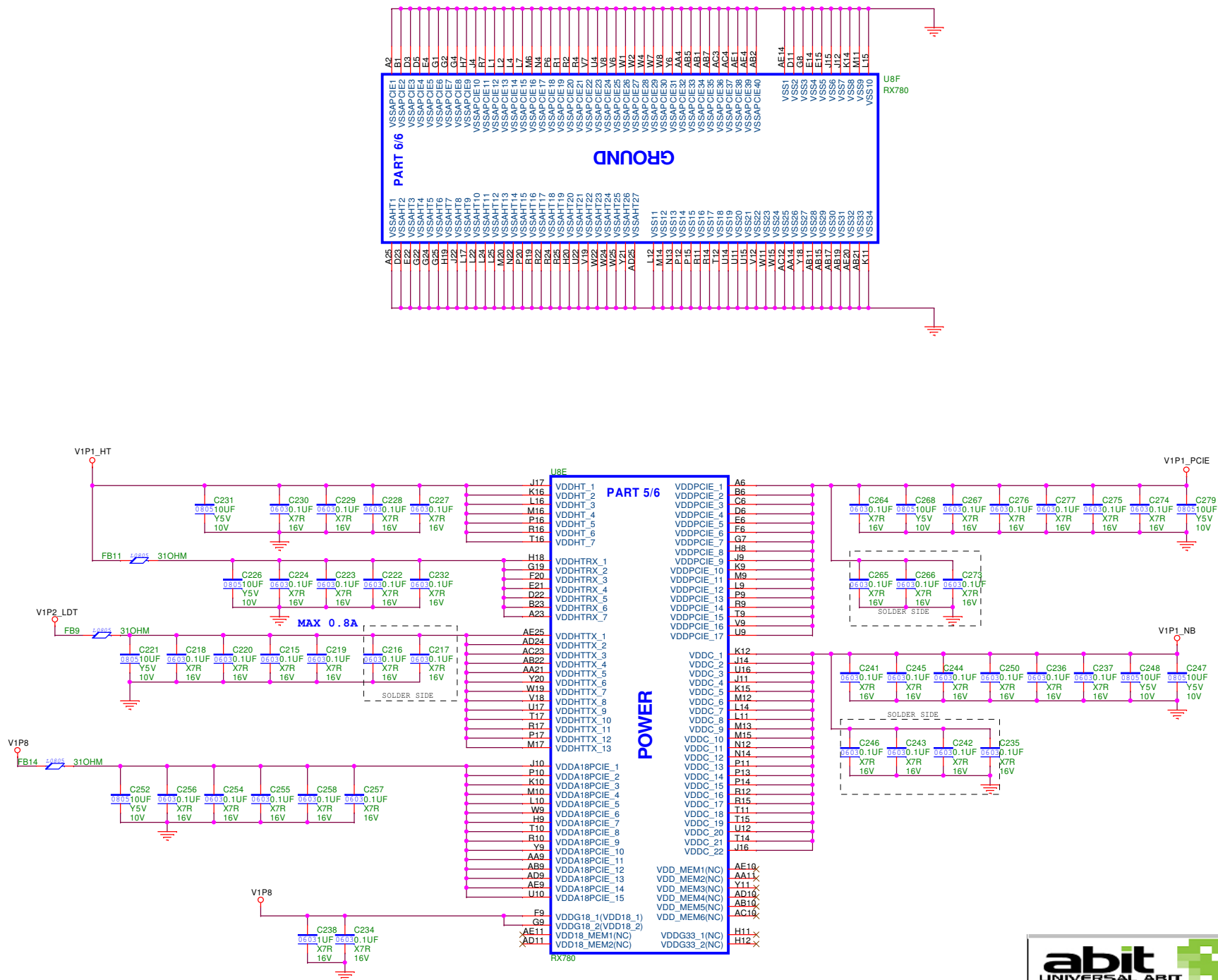


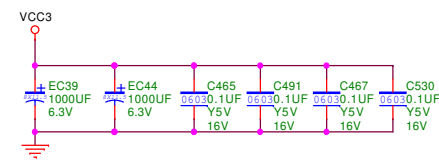
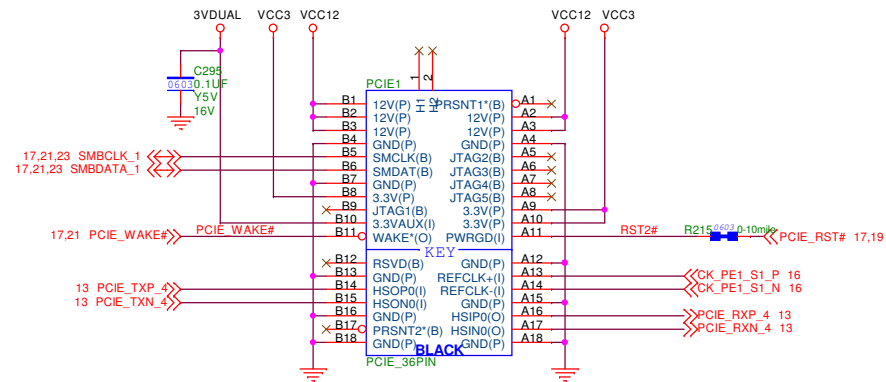
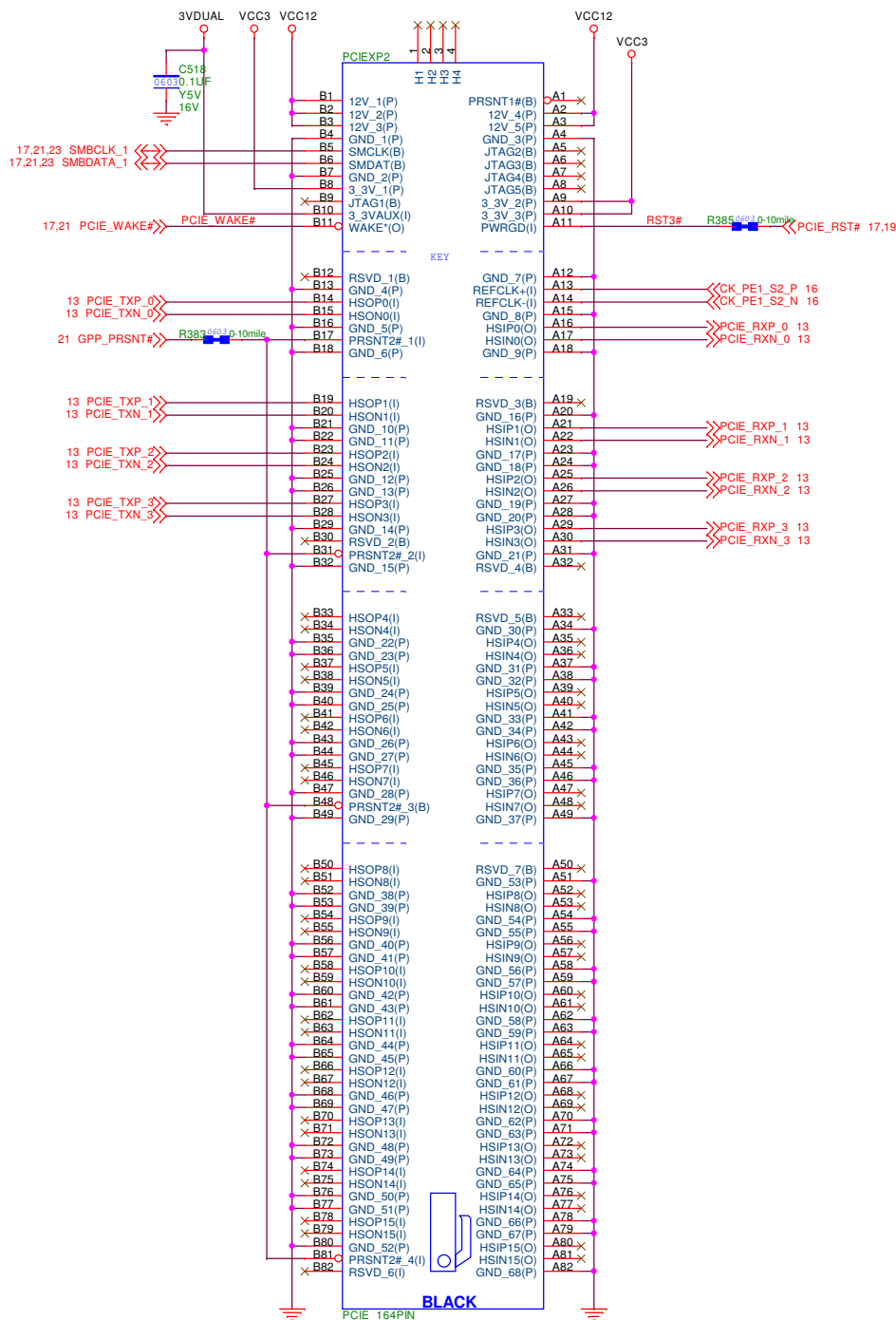


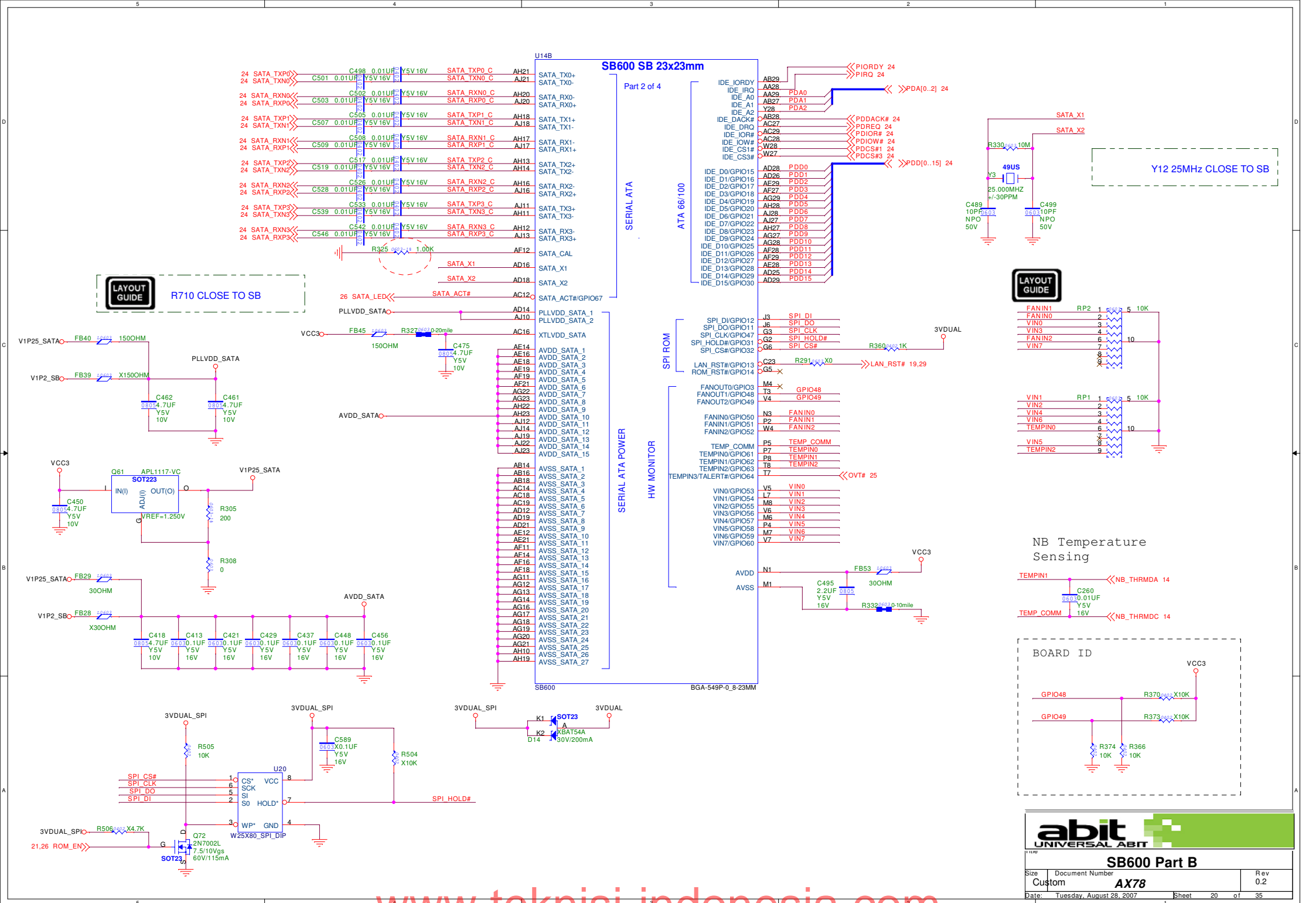
LVDS_DIGON, LVDS_BLON, LVDS_BLEN, STRP_DATA AND TMDS_HPD CAN BE CONFIGURED AS PWM OUTPUT

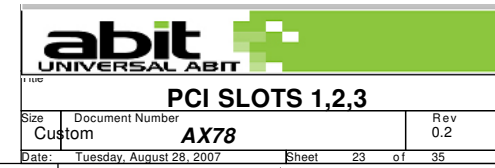
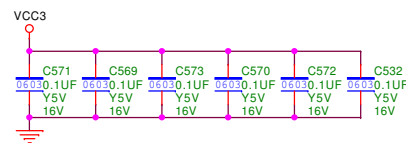
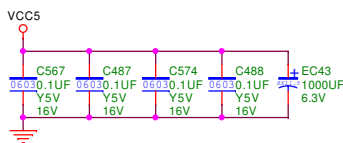
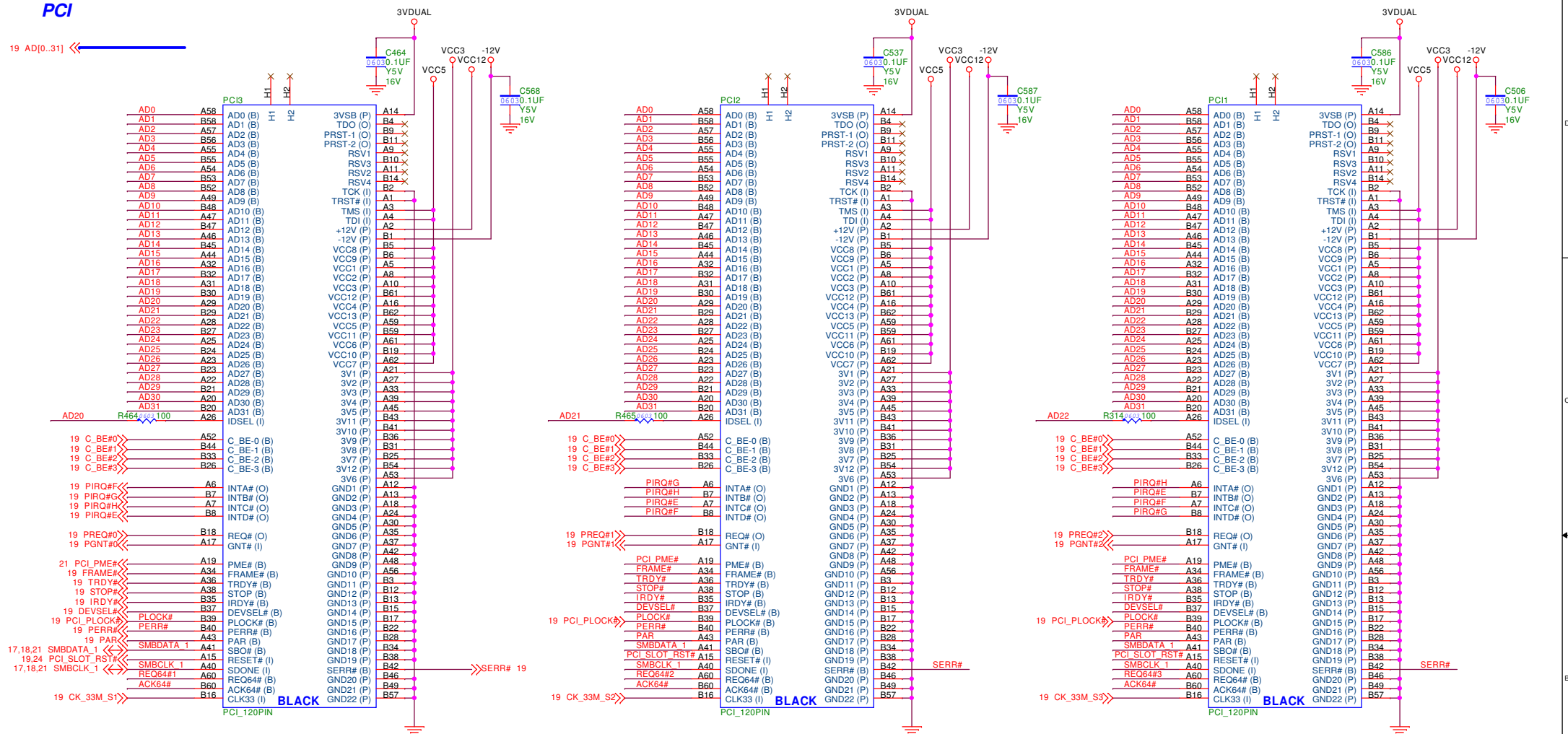


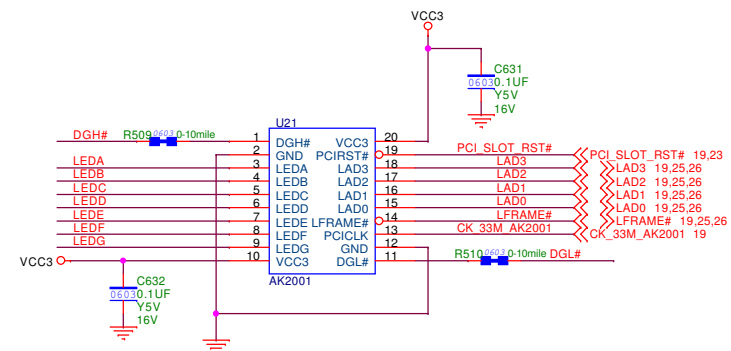
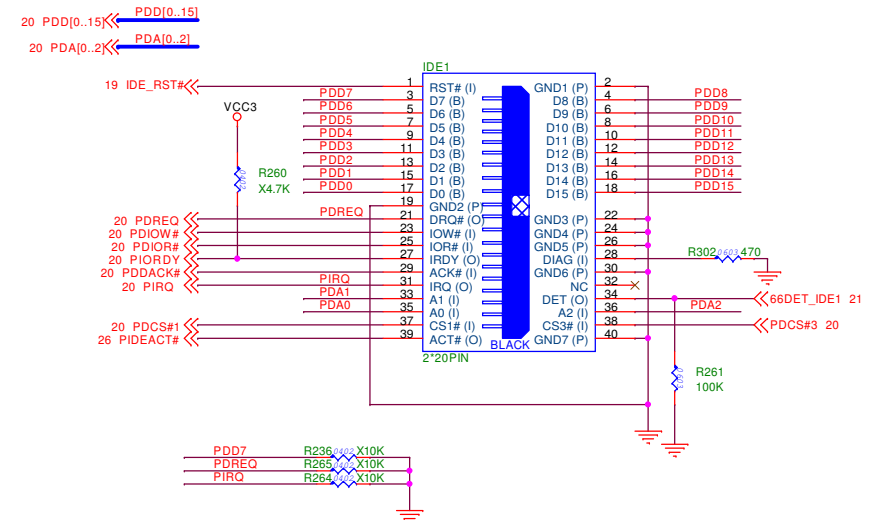
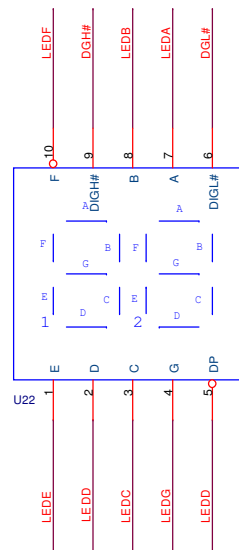
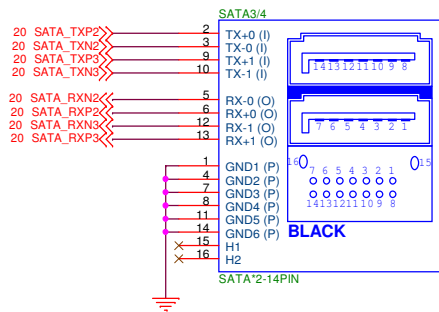
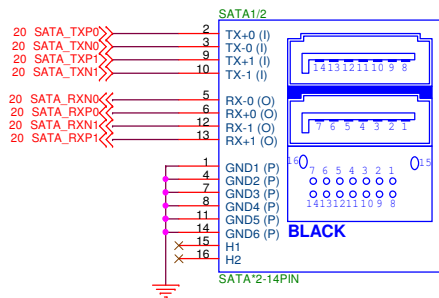
	RX780	RS690 only (NC for RS485)		
	DFT_GPIO1	DFT_GPIO0	DFT_GPIO[4:2]	DFT_GPIO5
PULL HIGH (internally pulled high)	Bypass the loading of EEPROM straps and use Hardware default values DEFAULT	Memory side port not available DEFAULT	These pin straps are used to configure PCI-E GPP mode: 111: register defined (register default to Config E) DEFAULT 110: 4-0-0-0-0 Config A 101: 4-4 Config B 100: 4-2-2 Config C 011: 4-2-1-1 Config D 010: 4-1-1-1-1 Config E others: register defined (register default to Config E)	Enable debug bus via the memory IO pads, if available in the package use default values DEFAULT
PULL LOW	I2C Master can load strap values from EEPROM if connected, or use default values if not connected	Memory side port available		use the memory data bus to output the debug bus



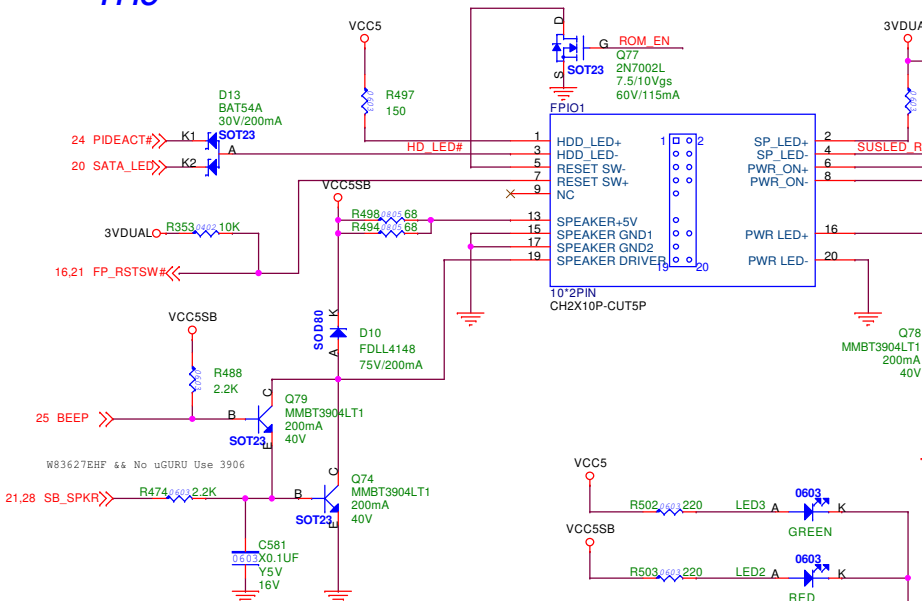




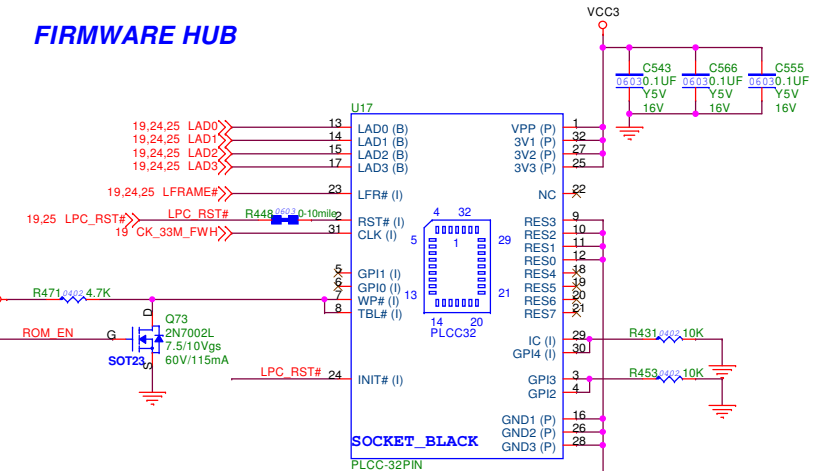




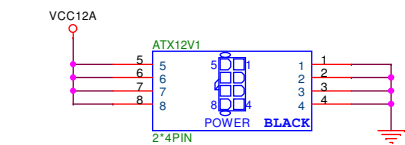
FPIO



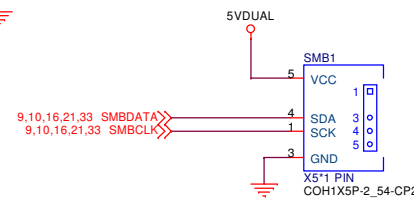
FIRMWARE HUB



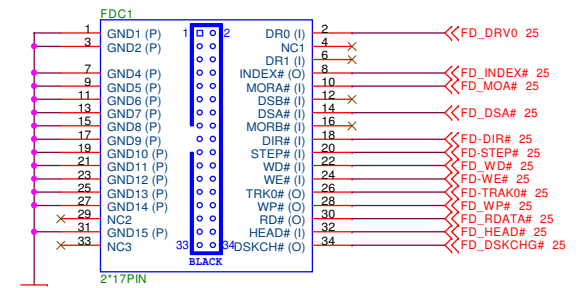
ATX POWER CONNECTOR

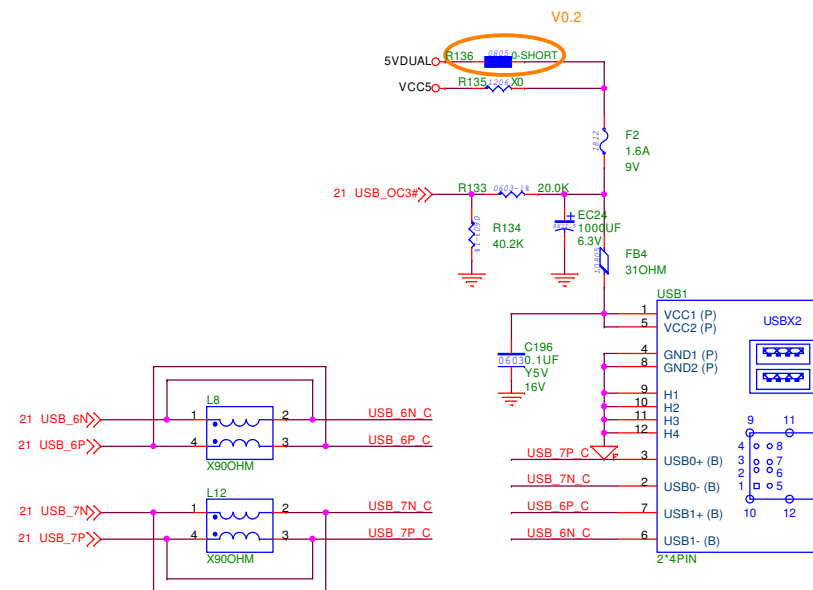
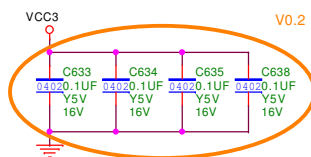


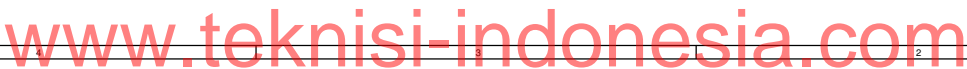
SM BUS



FDC

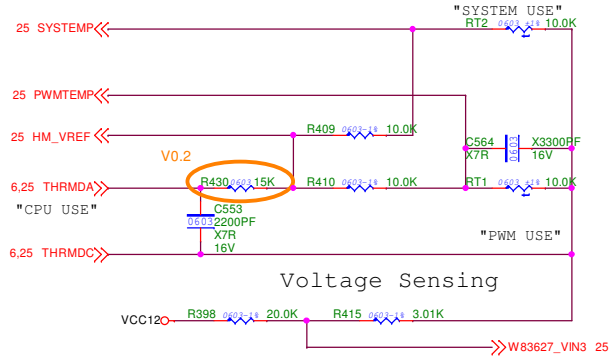




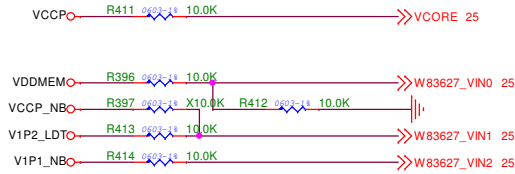


HW MONITOR

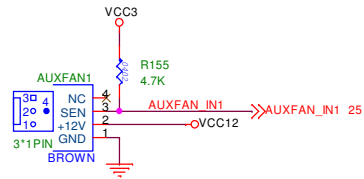
Temperature Sensing



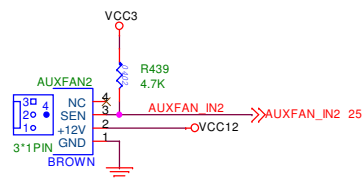
Voltage Sensing



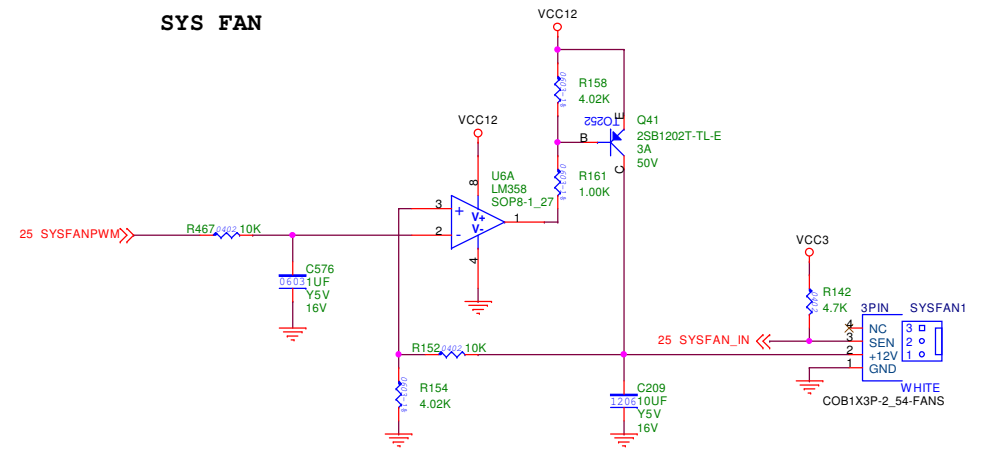
AUX FAN 1



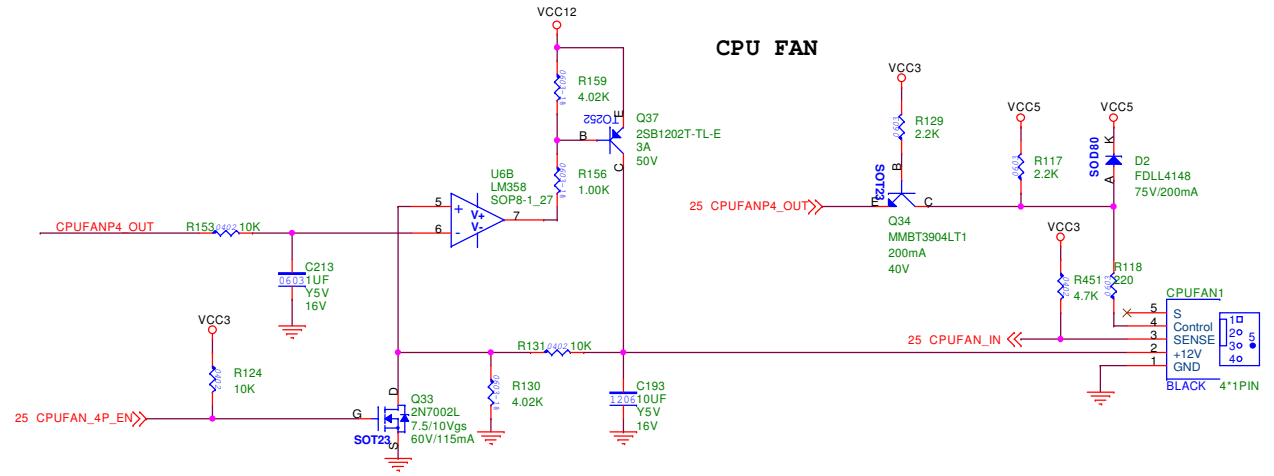
AUX FAN 2



SYS FAN



CPU FAN



CPU CHANGE

